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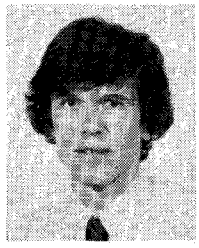

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Computer Calculation of Large-Signal GaAs FET Amplifier Characteristics

ANDRZEJ MATERKA AND TOMASZ KACPRZAK

Abstract—**A simple and efficient method of GaAs FET amplifier analysis is presented. The FET is represented by its circuit-type nonlinear dynamic model taking into account the device's main nonlinear effects including gate–drain voltage breakdown. An identification procedure for extraction of the model parameters is described in detail and examples are given. The calculation of the amplifier response to a single-input harmonic signal is performed using the piecewise harmonic balance technique. As this technique is rather time-consuming in its original form, the optimization routine used to solve the network equations was replaced by the Newton–Raphson algorithm. Characteristics calculated with the use of the proposed method are compared with experimental data taken for a microwave amplifier using a 2SK273 GaAs FET unit. Good agreement at 9.5 GHz over wide ranges of bias voltage and input power levels are observed.**

I. Introduction

THE GaAs FET is receiving continuously growing attention from circuit designers both in low-noise and high-power applications. Particularly, the power FET is an attractive device for use in microwave amplifiers and oscillators with its efficiency and power performance comparable or even superior to the other commercial solid-state or TWT sources. On the other hand, the power FET has received much less attention from researchers than its low-noise counterpart and, still, there is a need for data on device RF characterization at large-signal drive levels.

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Some efforts have been made to simulate the large-signal GaAs MESFET performance based on the numerical solution of the two-dimensional nonlinear differential equations describing the electron transport in the channel. The numerical results [1] are very helpful to understand device operation, but long computational time makes this approach impractical in circuit analysis and design programs. Recently, Madjar and Rosenbaum [2], [3] and Shur and Eastman [4] developed approximate analytical theories to model the active region under the gate of the microwave GaAs FET. Although one of these theories has been applied to the analysis of a practical microwave FET oscillator [3], both of them are of limited use in circuit design practice because they utilize the FET physical parameters which are scarcely available to the circuit designers. Willing, Rauscher, and de Santis [5] characterized an actual device with a quasi-static approach by measuring small-signal scattering parameters at a number of operating points to formulate an equivalent circuit, some of whose elements are bias-dependent. They use polynomial forms to approximate these dependences and a time-domain analysis program to calculate the large-signal device characteristics. The results obtained compare favorably with the experimentally determined characteristics, but the complexity of the equivalent circuit makes the identification technique of the model parameters rather laborious. Later, Rauscher [6]

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proposed an FET macromodel with a "lumped" nonlinearity, making it possible to analytically determine the optimum large-signal operating conditions of the FET in an oscillator circuit. A drawback of this approach is that the calculated optimum corresponds to a given combination of bias voltages. To achieve the circuit optimization over the entire range of the gate and drain voltages, one should perform a large number of measurements at elevated drive levels.

An alternative approach to the large-signal characterization of the microwave GaAs FET was used in the work of Tajima *et al.* [7]. They postulate that the large-signal device properties are governed primarily by the transistor dc characteristics—an assumption which has been verified at least up to 10 GHz. The Tajima model does not represent, however, the voltage-breakdown phenomenon [8] in the gate–drain region which is believed to have an impact on the FET gain saturation characteristics [9]. In order to take full advantage of the power capabilities of GaAs MESFET's, the breakdown effect is taken into account in the circuit-type large-signal dynamic model proposed in this paper.

The general problem of the microwave FET amplifier analysis is to derive a systematic procedure for defining the optimum input power, bias conditions, and terminating impedances that correspond to the maximum efficiency or output power at a given frequency. This can be facilitated greatly with the use of a computer and an appropriate large-signal analysis program. The computational task is to find a periodic steady-state response of a nonlinear network (i.e., the FET and its embedding circuit) to a single-input harmonic signal. The general-purpose time-domain analysis programs are not suitable for this aim because they are very time-consuming when applied to microwave circuits which typically consist of linear elements with a relatively small number of nonlinear ones. Additional difficulty arises from the fact that the time-delay effects as, e.g., the time difference between the changes in gate voltage and the relevant changes in the drain–source conduction current in the MESFET device, cannot be easily simulated with most time-domain analysis programs [10]. Another analysis method, of the simple iteration type, was applied by Tajima *et al.* [7] to the FET amplifier and oscillator design but sometimes it fails to converge, especially at high-input levels [11]. It follows then that the most efficient methods of proven value in the steady-state large-signal analysis of nonlinear circuits are the so-called piecewise harmonic balance techniques [12]. The network analyzed by these methods is decomposed into a minimum number of linear and nonlinear subnetworks and only frequency domain solutions of the linear subnetworks are required. In the original work of Nakhla and Vlach [12], an optimization procedure was used to solve the networks equations; however, it appears to be time-consuming and exhibits convergence problems at the high number of variables in the optimization process [13]. Taking the above considerations into account, the harmonic balance technique together with the Newton–Raphson method and appropriately formulated network equations [14] are used in the present work.

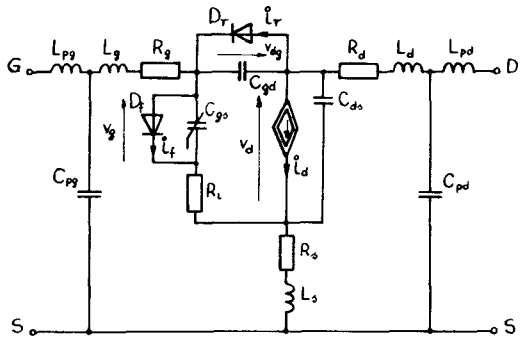

Fig. 1. FET large-signal equivalent circuit.

II. Large-Signal Dynamic GaAs MESFET Model

It was assumed, based on experimental study of arbitrarily selected transistors, that the main nonlinear elements of the model (see Fig. 1) are as follows [15]:

1) the equivalent gate-to-source capacitance C_{gs},
2) the diode D_f, which represents the current in the gate-to-channel junction,
3) the drain current source i_d controlled by voltage variables v_g and v_d,
4) the diode D_r, which represents the effect of the gate–drain breakdown. The diode parameters are not chosen to describe physical phenomena but to provide the best average fit to the experimental breakdown characteristics. The remaining parameters of this model are linear with their usual physical interpretation [16].

The nonlinear gate-to-source capacitance is given by

$$C_{gs} = C_{go}\left(1 - \frac{v_g}{V_{bi}}\right)^{-0.5}, \qquad \text{for } v_g < 0.8\, V_{bi} \tag{1}$$

and for $v_g \geqslant 0.8\, V_{bi}$ the plot of $C_{gs}(v_g)$ is approximated by a straight line with the slope equal to derivative dC_{gs}/dv_g obtained from (1) at $v_g = 0.8\, V_{bi}$. The parameters that appear in (1) are C_{go}, the gate-to-source capacitance for $v_g = 0$, and V_{bi}, the built-in potential of gate function.

The current of the diode D_f is given by

$$i_f = I_s\left[\exp(\alpha_s v_g) - 1\right] \tag{2}$$

with the model parameters I_s and α_s.

The voltage-controlled current source i_d is described by the formulas [17]

$$i_d = I_{dss}\left(1 - \frac{v_g}{V_p}\right)^2 \tanh\left(\frac{\alpha v_d}{v_g - V_p}\right) \tag{3}$$

$$V_p = V_{po} + \gamma v_d \tag{4}$$

where I_{dss}, V_{po}, α, and γ are the model parameters. In order to take into account the time delay between drain current and gate voltage, the instantaneous current $i_d(t)$ is calculated from (3) with $v_g = v_g(t - \tau)$ and $v_d = v_d(t)$, where τ is the model parameter.

The gate–drain breakdown effect is modeled by means of the diode D_r. The validity of such an approach was deduced from results of the two-dimensional computer simulation [18] and from dc breakdown characteristics measured for the transistors of various types, e.g., 2N6680 and 2SK273. The current in the diode D_r is given by

$$i_r = I_{sr}\left[\exp(\alpha_{sr} v_{dg}) - 1\right] \tag{5}$$

where I_{sr} and α_{sr} are the model parameters. It should be emphasized that the diode D_r does not represent any forward-biased p-n or Schottky-barrier junction connected between the gate and drain terminals. Instead, the current in the diode D_r approximates the breakdown current. For this reason, the parameters I_{sr} and α_{sr} in (5) are quite different in their values from the corresponding parameters I_s and α_s in (2). As a consequence, for small and moderate gate–drain voltages (e.g., up to 5 V for low-power FET's) and negative gate–source voltages, the gate current as calculated from (5) is negligibly small. However, it increases considerably at larger gate–drain voltages.

III. Determination of the Model Parameters

The model is characterized by a set of 24 parameters. Some of them are calculated from simple dc measurements, while others are fitted to dc and ac characteristics.

The parasitic source and drain resistances R_s and R_d can be determined by dc current and voltage measurements. R_s is found by passing a forward current I_G into the gate-source junction and measuring the resulting voltage at the floating drain with respect to the source [19]

$$R_s = \frac{\Delta V_{DS}}{\Delta I_G} \tag{6}$$

where ΔV_{DS} and ΔI_G are the incremental values of drain-source voltage and gate current, respectively. As the resistance R_s depends slightly on the gate current I_G, the average value obtained over a wide range of current can be used. Similarly, resistance R_d is found by forward biasing the gate–drain junction and measuring the voltage at the floating source.

The gate resistance R_g can be estimated from the measured I–V characteristic of the gate-source real Schottky diode

$$V_{GS} = I_G R + \frac{1}{\alpha_s} \ln \frac{I_G}{I_s} \tag{7}$$

where R is the series diode resistance and I_s, α_s are the parameters of (2). When $I_G R \ll \alpha_s^{-1} \ln(I_G/I_s)$, i.e., for low forward current I_G, the V_{GS} can be approximated by a second term on the right side of (7). The parameters I_s and α_s can then be obtained from the linear portion of the plot $\ln I_G$ versus V_{GS}. Substituting the values of I_s and α_s into (7), one can find the value of R from the $I_G - V_{GS}$ plot at high gate currents. Next, the gate-metalization resistance R_g is estimated as in [19]

$$R_g = \frac{R - R_s}{3}. \tag{8}$$

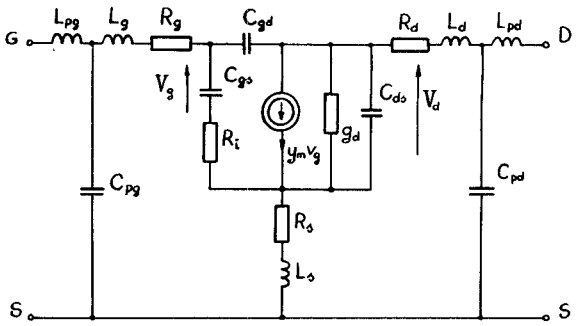

Fig. 2. FET small-signal equivalent circuit.

It was found from measurements that for gate-source voltage range $V_{GS} < V_p$ (the channel is pinched off regardless of drain-source voltage) the gate-drain breakdown current increases exponentially with increasing drain bias, and the breakdown characteristic does not depend on the voltage V_{GS}. Plotting $\ln i_r$ versus gate–drain voltage V_{DG}, one can obtain the parameters α_{sr} and I_{sr}.

The parameters I_{dss}, V_{po}, α, and γ are computer optimized to fit the dc $I_D - V_{DS}$ characteristics calculated from (3) and (4) to the measured ones in the triode and pentode regions, from zero up to breakdown voltage. Knowing the values of R_s and R_d, the internal voltages v_g and v_d can be calculated for each pair of external voltages V_{GS} and V_{DS} by means of the Newton–Raphson method—it needs about 3–4 iterations for a given accuracy of 1 μV. The maximum error of this global fitting did not exceed a few percent.

The remaining parameters of the FET model are determined using the small-signal equivalent circuit of the device shown in Fig. 2. The linear current source is described by the admittance

$$y_m = g_m \exp(-j\omega\tau) \tag{9}$$

where g_m is the transconductance at low frequencies. At the given quiescent operating point, the values of the transconductance g_m and the output conductance g_d are calculated as the drain current derivatives with respect to the gate-source voltage and drain-source voltage, respectively, with the drain current described by (3). Next, using these values of g_m and g_d together with the previously obtained values of R_s, R_d, and R_g, the remaining model parameters can be obtained by means of the computer fitting of the calculated S-parameters to the measured data in a prescribed frequency range [20].

The set of MESFET model parameters determined for a Mitsubishi 2SK273 unit (maximum total power dissipation at 25°C ambient, $P_T = 300$ mW) using the identification procedure as described above is given in Table I. The S-parameters were measured in the frequency range of 2–10 GHz at the bias voltages of $V_{GS} = -0.75$ V and $V_{DS} = 4$ V, which correspond nearly to the maximum power-added efficiency. The value of built-in voltage V_{bi} was assumed equal to 0.8 V. Fig. 3(a) shows the measured dc $I_D - V_{DS}$ output characteristics of the FET used for extraction of the model parameters I_{dss}, V_{po}, α, and γ, while in Fig. 3(b) are shown the calculated characteristics

TABLE I
MODEL PARAMETERS FOR A 2SK273 MESFET DEVICE

R_s [ohm]	4.5	I_{dss} [mA]	75.0	L_s [nH]	0.1
R_d [ohm]	4.5	V_{po} [V]	-1.78	L_d [nH]	0.2
R_g [ohm]	4.5	α [-]	3.35	L_g [nH]	0.2
R_i [ohm]	10.0	γ [-]	-0.11	τ [ps]	5.0
α_s [V^{-1}]	23.0	C_{go} [pF]	0.64	C_{pg} [pF]	0.26
I_s [nA]	1.05	V_{bi} [V]	0.80	C_{pd} [pF]	0.20
α_{sr} [V^{-1}]	1.28	C_{dg} [fF]	26.0	L_{pg} [nH]	0.67
I_{sr} [nA]	6.50	C_{ds} [pF]	0.10	L_{pd} [nH]	0.61

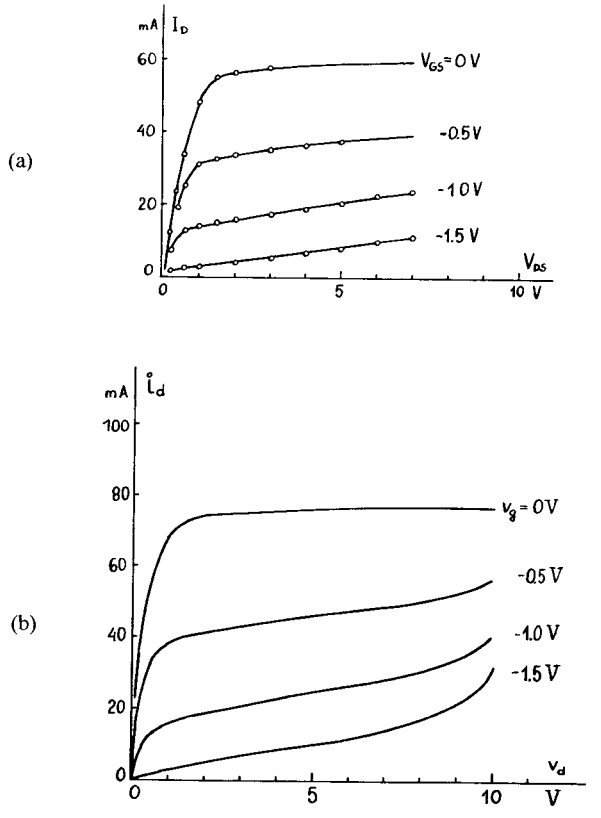

Fig. 3. (a) Measured (○○○) and calculated (———) dc characteristics of a 2SK273 unit. (b) Calculated characteristics of the internal transistor, including breakdown effects.

of the internal transistor including the voltage-breakdown effect.

IV. FET AMPLIFIER ANALYSIS

A simplified block diagram of the FET amplifier under consideration is shown in Fig. 4(a) where $Z_o = 50\ \Omega$, typically. One of the most important characteristics of the FET, which describes the power-handling capability of the device at a given frequency, is the dependency of the power delivered to the load P_o on the input power P_i. This is the so-called gain-saturation characteristic (often used in practical design procedures [6], [21]) which is measured with the input and output tuners adjusted for maximum P_o at a

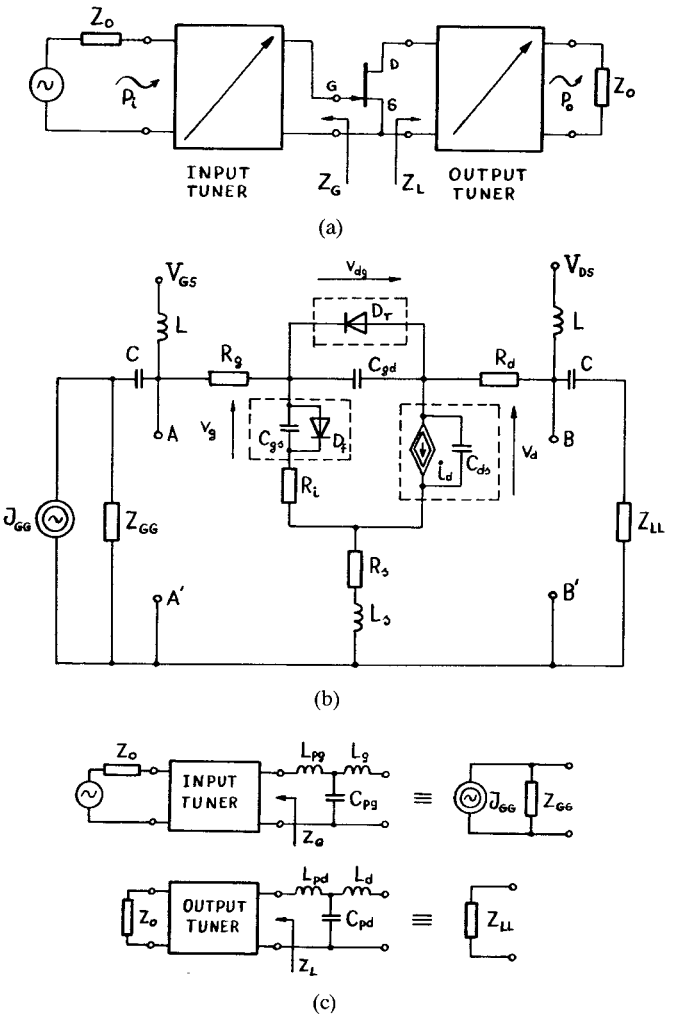

Fig. 4. (a) Simplified block diagram of an FET amplifier. (b) Large-signal equivalent circuit of the amplifier. (c) Equivalent transistor terminating circuits.

given P_i. To simulate this with the digital computer, the MESFET model proposed in this paper was used. After combining these linear and lossless elements of the model that represent gate and drain parasitics with the impedances Z_G and Z_L seen at the transistor terminals (see Fig. 4(a)) one obtains a simplified equivalent circuit of the amplifier as shown in Fig. 4(b). Dummy elements L and C in Fig. 4(b) represent, respectively, an open and short circuit at the signal frequency. V_{GS} and V_{DS} are the bias voltages, Z_{GG} and Z_{LL} are, respectively, the equivalent input and output terminating impedances. Their values can be easily calculated once the FET parasitics and the impedances Z_G and Z_L are measured (see Fig. 4(c)). J_{GG} stands for the input signal equivalent source.

For given values of frequency, J_{GG}, Z_{GG}, and Z_{LL}, one can calculate the response of the circuit of Fig. 4(b) using the harmonic balance technique. For its implementation, three nonlinear subnetworks were extracted from the amplifier equivalent circuit. These are shown inside the dashed boxes in Fig. 4(b). The Fourier coefficients of $v_g(t)$ and $v_d(t)$ have been chosen as independent variables in the harmonic balance routine [14]. The voltage $v_{dg}(t)$

was expressed in terms of v_g and v_d using Ohm's and Kirchhoff's laws.

Having the fundamental components of v_g and v_d one can calculate the input power at the terminals $A-A'$ (see Fig. 4(b)) and the output power at $B-B'$. Since the tuners' circuits and FET parasitics have been assumed lossless, these powers are equal to P_i and P_o, respectively. In order to calculate the power gain saturation characteristics, an optimization procedure was employed to find, for every given value of P_i, the values of Z_{GG} and Z_{LL} that correspond to the maximum of P_o. An objective function was defined as

$$E = \text{abs}(P_i - P_i^x) + \text{abs}(K - P_o^x) \qquad (10)$$

where P_i is the power available from the signal source, P_i^x is the actual power delivered to the amplifier input, K is a constant higher than any expected output power level, and P_o^x is the actual power delivered to the load. Obviously, the quantities P_i^x and P_o^x in (10) depend on the terminating impedances and the objective function has its minimum that corresponds to the impedances that match simultaneously both the input and output ports of the FET. A program was written to calculate the power gain saturation characteristics using the HP 9825A desk computer. A modified Davies–Swann–Campey direct-search minimization procedure [13] and the modified harmonic balance technique [14] were implemented in the program which occupies about 15k bytes of the computer memory.

V. Results

To calculate the power gain characteristics of the 2SK273 FET unit, the model parameters already specified in Section III are used. The parameters have been determined from the static I-V characteristics and from the small-signal S-parameters measured at the frequencies up to 10 GHz. On the other hand, the input signal frequency is chosen $f = 9.5$ GHz in the present example. Then, the model validity is not checked at the harmonic frequencies. Therefore, in the final analysis, only the dc component and the fundamental harmonic were used. However, this simplification does not generate a significant error, at least when the large-signal characteristics of an FET tuned amplifier are concerned, as can be seen later. The Newton–Raphson algorithm combined with the harmonic balance method [14] requires 4–10 iterations to calculate the amplifier voltage response with an error less than 1 mV, depending on the input power level. It takes about 10 min of the HP 9825A computer time to find values of Z_{GG} and Z_{LL} that match the simulated amplifier at a given value of P_i.

In Fig. 5 are shown the calculated power saturation characteristics obtained for the impedances Z_{GG} and Z_{LL} matching the transistor at every given input power P_i. The calculations were performed for $V_{DS} = 4$ V and two values of gate-source voltage: $V_{GS} = -0.75$ V and $V_{GS} = -1.25$ V. For input power $P_i \geq 5$ mW, the decrease in the transistor power gain is accompanied by a dc gate current flow, as it is seen in Fig. 5. This current consists of two components.

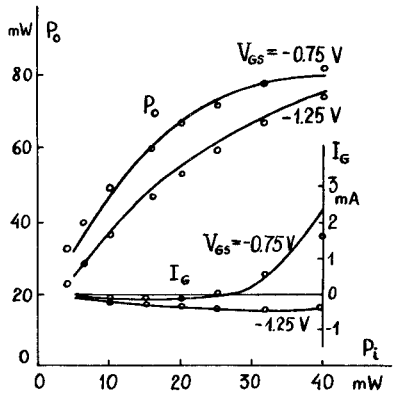

Fig. 5. Output power P_o and dc gate current I_G versus input power P_i. Measurements (○○○), calculations (———), $f = 9.5$ GHz, and $V_{DS} = 4$ V.

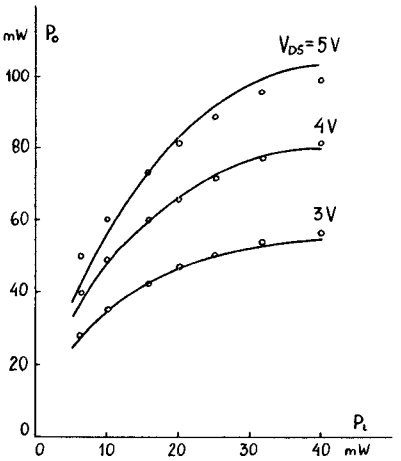

Fig. 6. Measured (○○○) and predicted (———) power-saturated characteristics, $f = 9.5$ GHz and $V_{GS} = -0.75$ V.

The negative component represents the breakdown effect while the positive one is due to the forward conduction of the gate junction [22]. In the case of $V_{GS} = -0.75$ V and small input power levels, the breakdown current dominates the forward conduction component, while for larger powers ($P_i \geq 30$ mW) the forward conduction is prevailing. In the case of $V_{GS} = -1.25$ V, in the whole range of input power up to 40 mW, the dc gate current is negative. Also shown in Fig. 5 are the results of measurements obtained using a load-pull technique [23]. Good agreement between theory and experiment is observed for the FET bias conditions as described previously.

In Fig. 6 are shown the power saturation characteristics for $V_{GS} = -0.75$ V and three values of drain-source voltage $V_{DS} = 3$, $V_{DS} = 4$, and $V_{DS} = 5$ V. Some discrepancies between the calculated and measured data are observed for $V_{DS} = 5$ V. These are attributed to the simplified description of the breakdown phenomena in the FET model. Particularly, the dynamics of the breakdown mechanisms [24] must be included in the GaAs FET model. The mathematical model (5) is of an instantaneous nature, but in general the breakdown effects may have time delays associated with them.

For every given value of P_i there exists a set of FET terminating impedances that corresponds to a maximum

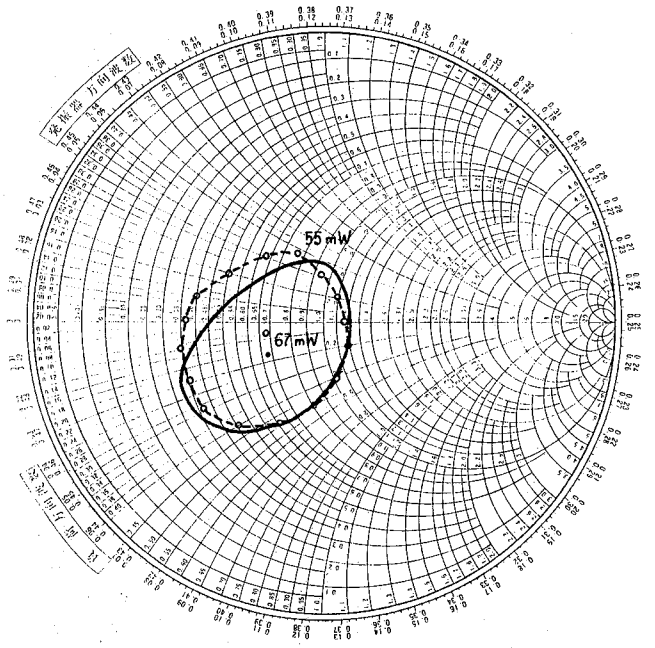

Fig. 7. Measured (○○○) and predicted (——) contours of constant output power on the load impedance plane, $Z_L/50\ \Omega$, $f = 9.5$ GHz, $V_{DS} = 4$ V, $V_{GS} = -0.75$ V, and $P_i = 20$ mW.

output power. Putting K in (10) less than this maximum value, one can calculate constant output power contours on the terminating impedances planes. These contours indicate how the output power of the FET varies as the function of the load impedance presented to it (see Fig. 4(a)). This information is very useful in designing practical amplifier and oscillator circuits. Measured and predicted contours of constant output power of the FET amplifier under consideration are shown in Fig. 7, for $P_i = 20$ mW, $V_{DS} = 4$ V, $V_{GS} = 0.75$ V, and the impedance Z_G (Fig. 4(a)) matching the amplifier's input. Considering the limited accuracy of impedance measurements at microwave frequencies, the agreement is very good.

VI. Conclusions

The reasonably simple and fairly accurate large-signal dynamic circuit-type model for a GaAs MESFET that is appropriate for use in circuit design programs has been proposed. The identification procedure of the model parameters is based on the experimental characterization of the FET dc current-voltage relationship and the frequency dependent small-signal S-parameters. The computer analysis of a large-signal X-band FET amplifier and the measurements of its performance have confirmed the validity of the model, in which only four elements were assumed to be nonlinear, i.e., C_{gs}, D_r, D_f, and i_d (see Fig. 1). These elements predominantly represent the power gain saturation of the transistor.

The model has been used to calculate the large-signal FET characteristics in the amplifier circuit with the use of a digital computer. The amplifier analysis method is based on the piecewise harmonic balance technique [12] with the originally recommended optimization procedure replaced by the Newton–Raphson computational scheme [14]. This modification considerably shortens the calculation time and enables us to perform an analysis and design process on the desk computer. Since nonlinear device operations as either power amplifiers and oscillators is quite similar, the FET characterization technique developed above for amplifiers can be readily carried over to meet oscillator design needs as well.

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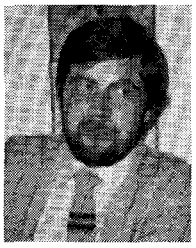

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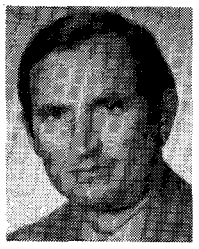

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Short Millimeter Wavelength Mixer with Low Local Oscillator Power

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Abstract—**This paper discusses development, for the 240-GHz region, of whisker contacted diode mixers with LO powers between 10 and 50 μW. Mixer requirements for low parasitic diodes, situated in high-embedding impedance circuits are described and appropriate RF and IF circuit designs presented. A capacitive post RF matching circuit for a full-height waveguide is developed with superior bandwidth characteristics at high impedance levels and greater ease of fabrication than usual matching circuits in reduced height guide. Corroborating experimental results are presented for an *X*-band model and for a 235-GHz mixer.**

I. Introduction

THE BEST MIXER performance within the 240-GHz region has been accomplished using whisker contacted Schottky barrier diodes situated in waveguide structures. The 1–10-mW LO power typically required for these fundamental mixers has usually been supplied by millimeter-wave tubes and more recently by a frequency tripled whisker contacted Gunn oscillator[1] with 2-mW output. Reduction of the LO power requirements to levels achievable with monolithic planar solid-state sources would simplify the system design and enhance the practicality of these mixers for tactical applications. This paper discusses the development of high-impedance room-temperature Schottky diode mixers with LO powers typically between 10 and 50 μW. Included in the paper are a) the analysis of the mixer under low LO power operation, b) the use of a novel capacitive stub impedance transformer to provide a high-embedding impedance diode mount in full-height waveguide, and c) experimental results for both an *X*-band simulating model and for a mixer operated at 235 GHz.

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[1] The 0.5-dB insertion loss was measured with a fixed 750-Ω resistor in place of the diode. This resistance is an average of diode resistance measurements taken previously without the IF matching circuit.

II. Diode and Circuit Requirements for Low LO Powers

The operation of mixer diodes at low LO power is conceptually no different than a mixer operating with the usual LO drive. In order to get efficient mixing, the LO voltage must be adequate to sweep the diode over a wide range of differential resistances. For millimeter-wave mixer diodes operating typically with ~1-mW LO drive, this

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